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METHOD AND APPARATUS FOR A COMPLEMENTARY ENCODER/DECODER

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METHOD AND APPARATUS FOR A COMPLEMENTARY ENCODER/DECODER

TECHNICAL FIELD

The invention relates generally to communications systems and, more particularly, to a method and an apparatus for encoding and/or decoding a bit message.

BACKGROUND

Digital networks generally involve the modulation of a bit stream on a transmitted signal. While providing for increased efficiencies, digital networks remain susceptible to noise, such as noise from buildings, trees, cars, electrical sources, magnetic sources, and the like. Typically, digital messages are encoded prior to modulation and transmission, and decoded upon reception and demodulation. The encoded digital messages are generally grouped into one or more bits forming a symbol. The symbol is used to select a high frequency sinusoidal electromagnetic (EM) wave that has been identified as representing the symbol. The technique generally used to transmit a symbol by a high frequency sinusoidal wave is to alter the wave's amplitude, frequency, and/or phase in a designated manner. Therefore, a wave comprising of a predetermined amplitude, frequency, and/or phase represents a symbol, *i.e.*, a predetermined bit pattern.

By transmitting digital messages in such a manner, it is possible to recover from some errors caused by noise in the transmission. The recovery of errors, however, is dependent upon an essentially random distribution of zeros and ones. Unfortunately, if a message comprises a substantial number of zeros, encoders and decoders generally provide poor results. Furthermore, a sequence of the same symbols in the transmission may fail other error correcting

function loops, such as a synchronization loop, an auto-gain control loop, and the like, since the function loops may need the differential information of the previously and the next received symbols to function properly.

Therefore, there is a need for a method and an apparatus for transmitting a digital message comprising a substantial number of zeros.

SUMMARY

The present invention provides a method and an apparatus for encoding and/or decoding a bit stream such that the encoded bit stream comprises zeros and ones. The encoding is accomplished by providing as input to a plurality of encoders differing versions, *i.e.*, containing a different sequence of corresponding bit values, of the bit stream. Similarly, the decoding is accomplished by accounting for the differing versions in the input to the decoder.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a diagram of a network environment that embodies features of the present invention;

FIGURE 2 is a block diagram illustrating one embodiment of the present invention in which a ones complementer is applied to a bit stream before encoding;

FIGURE 3 is a block diagram illustrating one embodiment of the present invention in which a bit stream is encoded using a Recursive Systemic Convolutional encoder;

FIGURE 4 is a Trellis diagram illustrating the state transitions of the encoder illustrated in FIG. 3; and

FIGURE 5 is a block diagram illustrating one embodiment of the present invention in which a bit stream is decoded.

DETAILED DESCRIPTION

In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be obvious to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block diagram form in order not to obscure the present invention in unnecessary detail. Additionally, for the most part, details concerning telecommunications and the like have been omitted inasmuch as such details are not considered necessary to obtain a complete understanding of the present invention, and are considered to be within the skills of persons of ordinary skill in the relevant art.

It is further noted that, unless indicated otherwise, all functions described herein may be performed in either hardware or software, or some combination thereof. In a preferred embodiment, however, the functions are performed by a processor such as a computer or an electronic data processor in accordance with code such as computer program code, software, and/or integrated circuits that are coded to perform such functions, unless indicated otherwise.

The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURES 1-5.

Referring to FIGURE 1 of the drawings, the reference numeral 100 generally designates a portion of a communications network which embodies features of the present invention. Specifically, the communications portion 100 comprises an encoder 112 configured to accept a source

bit stream 110 and to provide a transmitted code word 114 to a modulator 116. The source bit stream is generally organized into one or more frames, each frame comprising one or more bits. Typically, the source bit stream is organized into frames of hundreds or thousands of bits.

The modulator 116 is a digital modulator, such as a Quadrature Amplitude Modulator (QAM), Pulse Amplitude Modulation (PAM), Pulse Code Modulation (PCM), Differential Pulse-Code Modulation (DPCM), Phase-Shift Keying (PSK), Differential Phase-Shift Keying (DPSK), Offset Quadrature Phase-Shift Keying (OQPSK), Differential Quadrature Phase-Shift Keying ($\pi/4$-QPSK), Gaussian Filtered Minimum Shift Keying (GMSK), and the like, configured to convert the transmitted code word 114 into a transmitted modulated signal 118 that may be transmitted, as indicated by a transmission function 120.

The transmission function 120 is configured to provide the transmission of the transmitted modulated signal 118, via wireless or wireline technologies, resulting in the reception of a modulated signal 122. The transmission of signals via wireless or wireline technologies is well known to a person skilled in the art and, therefore, will not be discussed in greater detail, except insofar as is necessary to describe the present invention.

The received modulated signal 122 is provided to a demodulator 124 configured for converting the received modulator signal 122 into a received code word 126. The received code word 126 is provided as input to a decoder 128 configured for converting the received code word 118 into a received bit stream 130.

The encoder 120 and/or the decoder 128 may comprise of a stand-alone apparatus, an apparatus comprising an encoder

and/or decoder, such as a transmitter, a receiver, a mobile phone, and the like, or a module for an apparatus, such as a component of a transmitter, a receiver, a mobile phone, and the like. As such, the present invention should be construed to include apparatuses that are stand-alone encoders and/or decoders, apparatuses that comprise encoders and/or decoders, and modules comprising encoders and/or decoders.

It should be noted that noise in the transmission function 120 of the transmitted modulated signal 118 may prevent the reception of the received modulated signal 122 that is identical to the transmitted modulated signal 118. As a result, the demodulated signal, *i.e.*, the received code word 126, may differ from the transmitted code word 114. It is therefore preferred that the encoder 112 and the decoder 128 be configured to utilize a mechanism to help reduce the effect of noise and to assist in error recovery. One such mechanism that is particularly useful and commonly used in the industry is a turbo encoder/decoder utilizing a Recursive Systematic Convolutional (RSC) encoding technique. While the remaining discussion assumes, and provides examples for, the use of the RSC turbo encoder and decoder, the RSC turbo encoder and decoder are used for exemplary purposes only, and the present invention should not be limited to the use of the RSC turbo encoder and decoder. While other coding techniques, such as a Hamming code, a Golay code, a Reed-Muller code, a Bose, Chaudhuri and Hocquenghem (BCH) code, a Reed-Solomon code, a Fire code, a convolutional code, and the like, may be used with the present invention, studies have shown that turbo encoders comprising an RSC encoding technique generally outperforms other varieties, and, therefore, is the preferred method.

The use and operation of alternative encoder/decoder methods will be obvious to a person of ordinary skill in the art upon a reading of the present invention, and, accordingly, is to be included within the scope of the present invention.

FIGURE 2 exemplifies one embodiment of the encoder 112 (FIG. 1) that embodies features of the present invention, namely, a 1/5 rate turbo encoder, *i.e.*, every one input bit produces 5 output bits. While as mentioned above other encoders may be used in conjunction with the present invention, a turbo encoder is illustrated for the sake of conciseness.

The encoder 112 generally comprises multiplexing a systemic bit to two bits from each of two or more constitute encoders, which preferably utilize a Recursive Systematic Convolutional (RSC) encoding technique. Specifically, the encoder 112 is configured to comprise a first constitute encoder 210 and a second constitute encoder 212, each of which are explained in more detail below with reference to FIGURE 3.

The first constitute encoder 210 preferably accepts as input the source bit stream 110 (FIG. 1). Generally, the first constitute encoder 210 accepts a bit stream and outputs two bits, *i.e.*, a first constitute encoder (CE1) first bit 214 and a CE1 second bit 215, also known as parity bits, for each bit in the source bit stream 110.

The second constitute encoder 212 preferably accepts the source bit stream 110 that has been modified in order to prevent the first constitute encoder 210 and the second constitute encoder 212 from generating the same result, and to provide additional protection from noise. Preferably, the second constitute encoder 212 is configured to accept as input the source bit stream 110 after the source bit stream

110 has been encoded by an encoder ones complementer 222 and interleaved (*i.e.*, the order of the source bit stream 110 is essentially randomized) by an encoder interleaver 224, and to provide as output a second constitute encoder (CE2) first bit 216 and a CE2 second bit 217.

The encoder ones complementer 222 is configured to perform a ones complement function, *i.e.*, changing ones to zeros and zeros to ones. As can be seen below with reference to FIG. 3, the second constitute encoder 212 requires an input of one or more ones to generate a non-zero output. The encoder ones complementer 222 acts to insert ones into the transmitted code word 114 in a substantially random manner, thereby restricting the transmission of substantially all zeros, which is difficult to recover from noise-induced decoding errors. As exemplified below, an all-zeros bit stream is converted to a transmitted code word 114 comprising ones and zeros.

As mentioned above, the encoder ones complementer 222 may be replaced with another function that alters the bit stream such that the corresponding bit values are different, such as a differential encoder (the output is equal to the inverse of the exclusive or of the current bit and the previous bit). The purpose of the ones complementer 222, and the differential encoder, is to provide two different versions of the bit stream to at least two encoders. Any function providing this feature may be utilized. It should also be noted, however, that a corresponding modification must be made to the decoder 128.

The encoder interleaver 224 is configured to essentially randomize the order of the source bit stream 110 within each frame to reduce the effect of burst errors in the transmission. Generally, noise in a transmission

affects a series of contiguous bits, *i.e.*, burst errors, which are typically more difficult to recover from than corrupted, non-contiguous bits. The encoder interleaver 224 recognizes this phenomenon and attempts to dissipate the effect of noise by altering the order of the bits such that a burst error corrupting contiguous bits will be dissipated to non-contiguous bits when the bits are reordered upon reception, which will be discussed below with reference to FIGURE 5.

By way of example of the foregoing, in a block of 6 bits having bits 0, 1, 2, 3, 4, and 5 in sequential order, the encoder interleaver 224 may reorder the bits to be transmitted in the order 2, 5, 3, 1, and 4. A burst error corrupting two contiguous bits, such as 5 and 3, are reordered to their original bit positions upon reception, thereby dissipating the burst error to non-contiguous bits, limiting the effect of noise to non-contiguous bits and increasing the probability of recovering the corrupted bits. The design of the encoder interleaver 224 is dependent upon, among other things, the block size of the data and the anticipated signal-to-noise. The use and design of an interleaver is well known to a person of ordinary skill in the art, and therefore, will not be discussed in greater detail herein, except insofar as is necessary to describe the present invention.

A multiplexer 230 is configured to accept as input a systemic bit 213, which is the original, unmodified bit from the source bit stream 110, the CE1 first bit 214, the CE1 second bit 214, the CE2 first bit 215, and the CE2 second bit 216, and output the transmitted code word 114. The bits are preferably multiplexed using a straight bit-wise concatenation algorithm or a puncturing algorithm. The bit-

wise concatenation algorithm concatenates sequentially the systemic bit 213, the CE1 first bit 214, the CE1 second bit 215, the CE2 first bit 216, and the CE2 second bit 217, for each bit in the input bit stream.

Alternatively, a puncturing algorithm may be used to gain additional efficiencies by reducing the number of bits in the codeword 114. Puncturing is well known to a person of ordinary skill in the art and, therefore, will not be discussed in greater detail, except insofar as is necessary to disclose the present invention.

As will be appreciated by one skilled in the art upon a reading of the present invention, the encoder 112 is provided by way of example only and is not to be construed to limit the invention in any manner. For instance, additional constitute encoders may be used to provide additional data recovery, the encoder ones complementer may be implemented elsewhere, such as in conjunction with the first constitute encoder 210, the positioning of the encoder ones complementer 222 and the encoder interleaver 224 may be reversed, and the like. It should be noted, however, that making such modifications will require similar modifications to the decoder illustrated in FIG. 5, the modifications of which will be obvious to a person skilled in the art upon a reading of the present invention.

FIGURE 3 illustrates one method of performing the first constitute encoder 210 discussed above with reference to FIG. 2. The first constitute encoder 210 may also be used for the second constitute encoder 212 of FIG. 2.

Preferably, the first constitute encoder 210 comprises an RSC encoder with a memory of 3, as illustrated. The RSC encoder is illustrated for exemplary purposes only and is not to be construed as limiting the present invention in any

manner. It will be obvious to one skilled in the art upon a reading of the present invention that other designs of recursive or non-recursive, convolutional or block encoders are available and may be used in conjunction with the present invention, and, therefore, are to be included within the scope of the present invention.

Generally, the first constitute encoder 210 is configured with three memories, namely, a first memory 310, a second memory 312, and a third memory 314, also referred to as delays and/or shift registers. The first constitute encoder 210 is also configured to provide a recursive aspect to the encoding by applying the result of an exclusive or 316 of the value of the second memory 312 and the value of the third memory 314 to an exclusive or 318 with the input bit.

The output of the first constitute encoder 210 comprises a first bit 320, such as the CE1 first bit 214 and/or the CE2 first bit 216, and a second bit 322, such as the CE1 second bit 215 and/or the CE2 second bit 217. The first bit 320 is preferably the result of the exclusive or 326 of the result of the exclusive or 318, the first memory 310 and the third memory 314, and the second bit 322 is preferably the result of an exclusive or 324 of the result of the exclusive or 318, the first memory 310, the second memory 312, and the third memory 314.

FIGURE 4 is a Trellis diagram representation of the RSC encoding technique illustrated by the first constitute encoder 210 (FIG. 3) and is provided to further the understanding of the RSC encoding technique illustrated in the first constitute encoder 210 (FIG. 3). The Trellis diagram 400 represents a state diagram that illustrates the transition from a current state 410 to a new state 412.

Associated with each state "S0"-"S7" is a state value 414 comprising a three bit value that represents a state of the first memory 310, the second memory 320, and the third memory 314, respectively. Each possible transition is indicated by either a solid line or a dotted line. The dotted lines represent transitions from the current state 410 to the new state 412 as a result of the input bit being a "1," as illustrated by a "1" before the forward slash in the line label, and the solid lines represent transitions from the current state 410 to the new state 412 as a result of the input bit being a "0," as illustrated by a "0" before the forward slash in the line label.

Each line label also comprises two bits following the forward slash. The first bit represents the first bit from a constitute encoder, such as the CE1 first bit 214 and/or the CE2 first bit 216 of FIG. 2. The second bit represents the second bit from a constitute encoder, such as the CE1 second bit 215 and/or the CE2 second bit 217 of FIG. 2.

For example, if the current state 410 is "S0," then the first memory 310, the second memory 312, and the third memory 314 each contain a "0," as illustrated by the state value 414 of "S0=000." If, while in the current state 410 of "S0," the input bit is a "0," then the output of the first bit and the second bit of the first constitute encoder 210 are each "0," as indicated by the solid line between the current state 410 of "S0" and the new state 412 of "S0." Note that the line is labeled "0/00" because the input bit is a "0" and the output of the first and second bit of the RSC encoder were each "0." Upon transitioning into the new state 412 of "S0," the value of the first memory 310, the second memory 312, and the third memory 314 is "000," respectively, as indicated by the state value "S0=000."

If, however, while in the current state 410 of "S0," the systemic bit is a "1," then the output of the first bit 320 and the second bit 322 of the first constitute encoder 210 are each "1," as indicated by the dotted line between the current state 410 of "S0" and the new state 412 of "S4." Note that the line is labeled "1/11" because the input bit is a "1" and the output of the first bit 320 and the second bit 322 of the first constitute encoder 210 were each "1." Upon transitioning into the new state 412 of "S4," the value of the first memory 310, the second memory 320, and the third memory 314 is "100," respectively, as indicated by the state value "S4=100."

FIGURE 5 illustrates one method of performing the decoder 128 discussed above with reference to FIG. 1. Preferably, the decoder 128 comprises a turbo decoder as illustrated in FIG. 5. Specifically, reference numeral 128 is a turbo decoder that may be used to decode the received code word 126 as encoded by the turbo encoder as described in FIGS. 2-4. The turbo decoder, which is based on the Maximum A-Posteriori Probability (MAP) algorithm, is illustrated for exemplary purposes only and is not to be construed as limiting the present invention in any manner. It will be obvious to one skilled in the art upon a reading of the present invention that other designs of decoders, such as log-MAP, Max-log-MAP, Soft Output Viterbi Algorithm (SOVA), and the like, may be utilized, and, therefore, are to be included within the scope of the present invention.

Generally, as will be discussed in greater detail below, the decoder 128 comprises a first decoder 512 and a second decoder 518 operating serially in an interative manner. The output of the first decoder 512, *i.e.*, $L_e(12)$, is one of the inputs to the second decoder 518, and the

output of the second decoder 518, *i.e.*, $L_e(21)$, is one of the inputs of the first decoder 512. The first decoder 512 is responsible for decoding the bits encoded by the first constitute encoder 210 (FIG. 2), and the second decoder 518 is responsible for decoding the bits encoded by the second constitute encoder 212 (FIG. 2).

The decoder 128 comprises a demultiplexer 510 configured to demultiplex the received code word 126 (FIG. 1) into five bits, namely, a received systemic bit 502, a received first decoder (D1) first bit 504, a received D1 second bit 506, a received second decoder (D2) first bit 508, and a received D2 second bit 510, which correspond to the systemic bit 213, the CE1 first bit 214, the CE1 second bit 215, the CE2 first bit 216, and the CE2 second bit 217, respectively.

The first decoder 512 is configured to accept the received systemic bit 502, the D1 first bit 504, and the D1 second bit 506 as input. In addition to the three inputs listed above, the first decoder 512 is also configured to receive as input a natural log of the likelihood that the received systemic bit 502 is a one ($-L_e(21)$), where the notation of "(21)" indicates that the values are the results of the second decoder that are sent to the first decoder, and, similarly, "(12)" indicates that the values are the results of the first decoder that are sent to the second decoder. The ($-L_e(21)$) is initialized to zero and will be discussed in more detail below with reference to a sign inverter 526.

The first decoder 512 may be any decoding algorithm that provides satisfactory results for the type of encoder chosen. For instance, suitable decoding techniques for the turbo encoder illustrated in FIGS. 2-4 are the MAP, SOVA,

log-MAP, Max-log-MAP, and the like. The decoding techniques are well known to a person of ordinary skill in the art, and the interaction of the decoding technique with the present invention will be obvious to a person of ordinary skill in the art upon a reading of the present invention.

The first decoder 512 preferably provides output in the form of the natural log of the likelihood that a particular bit is a 1. Specifically, the output of the first decoder 512 is given by the following formula:

$$L_e(12) = \log e\left(\frac{p[received systemic bit = 1]}{p[received systemic bit = 0]}\right),$$

where:

p[received systemic bit = 1] is the probability that the received systemic bit 502 is equal to a 1; and

p[received systemic bit = 0] is the probability that the received systemic bit 502 is equal to a 0.

Therefore, $L_e(12)$ will be positive if there is a higher probability that the received systemic bit 502 is a one and will be negative if there is a higher probability that the received systemic bit is a zero.

As mentioned above, the output values of the first decoder 512 are input to the second decoder 518. The values, however, must be adjusted to account for the encoder ones complementer 222 (FIG. 2) and the encoder interleaver 224 (FIG. 2). As illustrated in FIG. 2, the first constitute encoder 210 received as input bits that were neither interleaved nor inverted, *i.e.*, ones complement. The second encoder 212, however, received as input bits that were reorder by the encoder interleaver 224 and inverted by the encoder ones complementer 222.

Therefore, referring now back to FIG. 5, the output of the first decoder 512 must be reordered by a first decoder interleaver 514 and sign inverted by a sign inverter 516. The result of the first decoder interleaver 514 and the sign inverter 516 is the probability that the received systemic bit 502 is a zero ordered in the same manner as the D2 first bit 508 and the D2 second bit 510.

Similarly, the received systemic bit 502 must be adjusted to provide the bits in the same order and the same inverted representation as used to generate the D2 first bit 508 and the D2 second bit 510, *i.e.*, duplicate the input to the second constitute encoder 212 (FIG. 2). As a result, a second decoder interleaver 520 and a decoder ones complementer 522 is applied to the received systemic bit 502.

Therefore, the input to the second decoder 518 comprises the ($-L_e(12)$), the received systemic bit 502 reordered and bit interverted, the D2 first bit 508, and the D2 second bit 510. The operation of the second decoder 518 is as described above with reference to the first decoder 512.

The second decoder 518 preferably provides output in the form of the natural log of the likelihood that a particular bit is a 1. Note that due to the ones complement function, a high probability result from the second decoder 518 that a bit is a 1 is actually a high probability result that the bit is a 0. Specifically, the output of the second decoder 518 is given by the following formula:

$$L_e(21) = \log e\left(\frac{p[invertedreceivedsystemicbit = 1]}{p[invertedreceivedsystemicbit = 0]}\right),$$

where:

p[inverted received systemic bit = 1] is the probability that the received systemic bit 502 after application of the decoder ones complement 522 is equal to a 1, *i.e.*, actually a 0; and

p[inverted received systemic bit = 0] is the probability that the received systemic bit 502 after application of the decoder ones complement 522 is equal to a 0, *i.e.*, actually a 1.

Therefore, $L_e(21)$ will be positive if there is a higher probability that the received systemic bit 502 is a zero and will be negative if there is a higher probability that the received systemic bit is a one.

As mentioned above, the output of the second decoder 518 is used as input to the first decoder 512. Similar to $L_e(12)$, however, the output $L_e(21)$ must be adjusted to account for the ones complement and interleaving functions. Therefore, a de-interleaver 524 and a second sign inverter 526 is applied to the output of the second decoder 518 prior to being used as input to the first decoder 512.

The turbo decoder process described above is preferably performed on the block of received bits for one or more iterations as determined by a decision unit 528. Preferably, the process is performed eight iterations. Alternatively, the decision unit 528 may be configured to vary the number of iterations based upon, among other things, the probabilities, the variance between iterations, and the like. Upon determining that the number of iterations is sufficient, the decoder 128 outputs the received bit stream 130 (FIG.1).

It should also be noted that the decoder ones complementer 522 may be replaced with a differential encoder

if a differential encoder is used in place of the encoder ones complementer 222 (FIG. 2) as mentioned above.

By way of example, suppose the source bit stream 110 comprises a stream of 42 zeros. The output of the encoder 112, assuming the absence of the encoder interleaver 224, is illustrated in the following table. The first row represents the transmitted code word, which comprises, in order, the systemic bit 213, the CE1 first bit 214, the CE1 second bit 215, the CE2 first bit 216, and the CE2 second bit 217. The second row represents the value of the systemic bit, which is always zero in this example.

The third row represents the output of the first constitute encoder 210 and, in parenthesis, the state transitions as illustrated in FIG. 4. Note that the first constitute encoder 210 outputs all zeros when the value of the systemic bit is zero and that the state transition is always from state "S0" to state "S0."

The fourth row represents the output of the second encoder 212 and, in parenthesis, the state transitions as illustrated in FIG. 4. Note that, due to the ones complement, the output is not always zeros. An input stream of 42 zeros will repeat this pattern six times.

Transmitted Code Word	00011	00000	00010	00001	00000	00001	00011
Systemic bit	0	0	0	0	0	0	0
First Encoder	00 (S0 to S0)	00 (S0 to S0)	00 (S0 to S0)	00 (S0 to S0)	00 (S0 to S0)	00 (S0 to S0)	00 (S0 to S0)
Second Encoder	11 (S0 to S4)	00 (S4 to S6)	10 (S6 to S3)	01 (S3 to S5)	00 (S5 to S2)	01 (S2 to S1)	11 (S1 to S0)

Therefore, if the modulator 116 (FIG. 1) that transmits 5 bits in each cycle, a zero will be assigned 4 different

values, namely, 0, 1, 2, and 3. Additional variations may be obtained by choosing a modulator 116 that transmits a different number of bits than the rate of the encoder (1/5 for this example), such as the 64 QAM, which transmits 6 bits per pulse.

For example, the following string comprises the above bit pattern concatenated together and divided into 6-bit blocks, as would be the case if a 1/5 rate turbo encoder were used in conjunction with 64 QAM.

000110 | 000000 | 010000 | 010000 | 000001
000110 | 001100 | 000000 | 100000 | 100000
000010 | 001100 | 011000 | 000001 | 000001
000000 | 000100 | 011000 | 110000 | 000010
000010 | 000000 | 001000 | 110001 | 100000
000100 | 000100 | 000000 | 010001 | 100011
000000 | 001000 | 001000 | 000000 | 100011

For ease of comparison, the following digital string replaces the binary string with their decimal equivalent.

6 | 0 | 16 | 16 | 1
6 | 12 | 0 | 32 | 32
2 | 12 | 24 | 1 | 1
0 | 4 | 24 | 48 | 2
2 | 0 | 8 | 49 | 32
4 | 4 | 0 | 17 | 35
0 | 8 | 8 | 0 | 35

Therefore, the use of the ones complement encoder/decoder enclosed in the present invention results in the use of 14 different symbols, *i.e.*, pulses, in a system

utilizing 64 QAM, namely, 0, 1, 2, 4, 6, 8, 12, 16, 17, 24, 32, 35, 48, and 49.

It is understood that the present invention can take many forms and embodiments. Accordingly, several variations may be made in the foregoing without departing from the spirit or the scope of the invention. For example, different encoding schemes may be utilized that provide different versions of the bit stream to a plurality of encoders.

Having thus described the present invention by reference to certain of its preferred embodiments, it is noted that the embodiments disclosed are illustrative rather than limiting in nature and that a wide range of variations, modifications, changes, and substitutions are contemplated in the foregoing disclosure and, in some instances, some features of the present invention may be employed without a corresponding use of the other features. Many such variations and modifications may be considered obvious and desirable by those skilled in the art based upon a review of the foregoing description of preferred embodiments. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.